QMB-12 The QUIET MOTHER_{TM}12 Slot Motherboard

Soldering PC Boards

Two common causes of trouble with PC boards are bad solder joints or solder bridges. Usually, bad solder joints are caused by either a cold solder joint or contamination. A good solder joint is characterized by a bright shiny and smooth surface (see figure 1).

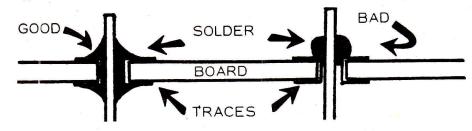
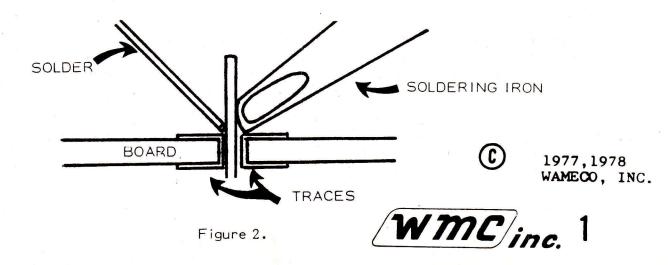


Figure 1. CROSS-SECTION OF A PC BOARD SHOWING GOOD AND BAD SOLDER CONNECTIONS

A cold solder joint is characterized by a dull surface and usually a lumpy or balled appearance. It takes practice and patience to obtain a good solder joint consistently. However, the first step is to apply flux to all connections before the solder. Second, heat the connection for a second or two with the soldering iron. Third, apply solder to the opposite side of the connection. Don't touch the solder to the iron. Flux has a "wetting" effect on solder which causes the solder to flow smoothly, completely filling the connection. If flux is not used or the metal around the connection is contaminated (dirty) it is almost impossible to have a good solder joint.

Solder bridges are usually caused by using a soldering iron tip that's too large, solder wire that's too large, or trying to rush the job. Use a small spade tip iron (see figure 2). Touch the connection with the flat side of the tip. After the flux bubbles, touch the solder to the opposite side of the connection. Again, don't touch the solder to the iron. The connection is hot enough to melt the solder causing it to flow around the connection. Do not use too much solder. Use a little and watch it flow. Solder is like spice for cooking, don't use too much.

Applying heat for extended periods will cause either or both of the following: the trace or pad will lift from the board or the board material will turn brown. Remove the iron before this happens. One hobbyist counts the bubbles that pop in the solder. He found seven to nine bubbles insured good solder flow without over heating.



The QMB-12 Motherboard is designed to conform with the S-100 (WAMECO_{TM}) bus (see figures 3A, 3B). In this bus there are 18 pins not otherwise used. These pins are available for non-standard configurations. It is advisable to carefully consider any modification since this will limit board usage to a modified system. If a full 12 connector system is not being made, put the connectors as close to the input connections as possible. The QMB-12 is shorter than many motherboards on the market. Therefore, it is possible that the QMB-12 will work without termination. Try to operate without termination. If satisfactory operation is obtained, don't terminate. The passive RC network that Wameco has designed is better than any active termination design on the market in that the network does not load the lines during static signal conditions. Place termination only on lines marked with X in figure 3A.

Parts List

| 100 pin connector (any brand that has 0.125" spacing between pins in a row and 0.250" spacing between rows) |
|--|
| 22 Ufd tantalum electrolytic capacitors |
| 0.01 Ufd disc or tubular capacitors |
| 120 Ohm 1/4 Watt carbon resistors |
| 320T-12 or 7912 negative 12 volt regulator |
| 340T-5 or 7805 positive five volt regulator |
| 340T-12 or 7812 positive 12 volt regulator |
| |

Tools and supplies needed for construction of QMB-12

- l Multimeter
- 1 25 Watt fine tip soldering iron
- 1 Bottle flux cleaner
- 1 Pair needle nosed pliers
- 1 Xacto knife
- 1 Pair diagonal cutting pliers
- 1 Bottle rosin soldering flux
- 1 Roll solder (rosin core 0.031" or 0.040" diameter)
- 1 Roll solder wick
- 1 Magnifying glass
- 1 Strong light

I. Assembly of QMB-12

I-1. Before placing any parts on the board, check the board for any hairline shorts (slivers). All boards have been checked at least three times before shipping. Still, a good hobbyist checks any board he buys.

I-2. Using a strong light and a magnifying glass, very carefully check all leads on the top of the board (this is the side marked "component side"). If any slivers are found, carefully cut and scrape them with an Xacto knife. The underside of the board will be checked after assembly.

I-3. Place the QMB-12 motherboard component side up so that the words "component side" are on lower left. Insert all appropriate 100 pin connectors. If less than 12 connectors are to be installed, place them in successive locations from left to right on the board.

S-100 (WAMECO) BUS DESCRIPTION

| 1 $+5V$ 2 $+15V$ 3 XRDY X 4 VIØ X 5 VII X 6 VI2 X 7 VI3 X 8 VI4 X 9 VI5 X 10 VI6 X 11 VI7 X 12 X X 13 X X 14 X X 15 X X 16 X X 17 X X 18 STAT DISABLE X 20 UNPROTECT X 21 SS X 22 ADDR DSBL X 23 DO DSBL X 24 Ø2 X 25 Ø1 X 26 PHLDA X 27 PWAIT Z 28 PINTE Z 29 A5 X </th <th></th> | |
|--|---|
| 7 $\nabla I3$ X 8 $\nabla I4$ X 9 $\nabla I5$ X 10 $\nabla I6$ X 11 $\nabla I7$ X 12 $I3$ $I4$ 15 $I4$ $I6$ 16 $I7$ $I6$ 17 $I6$ $I7$ 18STAT DISABLE X 19CIC DISABLE X 20UNPROTECT X 21SS X 22ADDR DSBL X 23DO DSBL X 24 $Q2$ X 25 $\emptyset1$ X 26PHLDA X 27PWAIT Z 28PINTE | |
| 7 $\sqrt{13}$ χ 8 $\sqrt{14}$ χ 9 $\sqrt{15}$ χ 10 $\sqrt{16}$ χ 11 $\sqrt{17}$ χ 1213141516171617181718STAT DISABLE19CIC DISABLE χ 20UNPROTECT χ 21SS χ 22ADDR DSBL χ 23DO DSBL χ 24 $\sqrt{2}$ χ 25 \emptyset 126PHLDA χ 27PWAIT28PINTE | |
| 7 $\sqrt{13}$ χ 8 $\sqrt{14}$ χ 9 $\sqrt{15}$ χ 10 $\sqrt{16}$ χ 11 $\sqrt{17}$ χ 1213141516171617181718STAT DISABLE19CIC DISABLE χ 20UNPROTECT χ 21SS χ 22ADDR DSBL χ 23DO DSBL χ 24 $\sqrt{2}$ χ 25 \emptyset 126PHLDA χ 27PWAIT28PINTE | |
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| 7 $\sqrt{13}$ χ 8 $\sqrt{14}$ χ 9 $\sqrt{15}$ χ 10 $\sqrt{16}$ χ 11 $\sqrt{17}$ χ 1213141516171617181718STAT DISABLE19CIC DISABLE χ 20UNPROTECT χ 21SS χ 22ADDR DSBL χ 23DO DSBL χ 24 $\sqrt{2}$ χ 25 \emptyset 126PHLDA χ 27PWAIT28PINTE | |
| 11VI7X121313141516161718STAT DISABLE19CIC DISABLE20UNPROTECT21SS22ADDR DSBLX2324 | |
| 12131415161718STAT DISABLE19CIC DISABLE20UNPROTECTX21SSX2ADDR DSBLX23DO DSBLX24 | |
| 13 14 14 15 16 17 18 STAT DISABLE 19 CIC DISABLE 20 UNPROTECT 21 SS 22 ADDR DSBL 23 DO DSBL 24 02 25 \$01 26 PHLDA 27 PWAIT 28 PINTE | |
| 1516161718STAT DISABLE19CIC DISABLE20UNPROTECT21SS22ADDR DSBL23DO DSBL24Ø225Ø126PHLDA27PWAIT28PINTE | |
| 15161718STAT DISABLE19CIC DISABLE20UNPROTECT21SS22ADDR DSBL23DO DSBL24Ø225Ø126PHLDA27PWAIT28PINTE | |
| 1718STAT DISABLEX19CIC DISABLEX20UNPROTECTX21SSX22ADDR DSBLX23DO DSBLX24Q2X25Ø1X26PHLDAX27PWAIT28PINTE | |
| 17 18 STAT DISABLEX 19 CIC DISABLEX 19 CIC DISABLEX 20 UNPROTECTX 21 SSX 22 ADDR DSBLX 23 DO DSBLX 24 02 X 25 01 X 26 PHLDAX 27 PWAIT 28 PINTE | |
| 18STAT DISABLEX19CIC DISABLEX20UNPROTECTX21SSX22ADDR DSBLX23DO DSBLX24Q2X25Ø1X26PHLDAX27PWAIT28PINTE | 1 |
| 19CIC DISABLEX20UNPROTECTX21SSX22ADDR DSBLX23DO DSBLX24Ø2X25Ø1X26PHLDAX27PWAIT28PINTE | |
| 19CIC DISABLEX20UNPROTECTX21SSX22ADDR DSBLX23DO DSBLX24Ø2X25Ø1X26PHLDAX27PWAIT28PINTE | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | 1 |
| 26PHLDAX27PWAIT28PINTE | 1 |
| 27PWAIT28PINTE | - |
| 28 PINTE | - |
| | - |
| | 4 |
| 30 A4 | - |
| | - |
| | 4 |
| | 4 |
| | - |
| | 4 |
| | _ |
| 36 DOØ X | _ |
| 37 A10 | _ |
| 38 DO4 X | - |
| 39 DO5 X | |
| 40 DO6 X | |
| 41 DI2 X 42 DI3 X | |
| 42 DI3 X | |
| 43 DI7 X | |
| 44 SMI | |
| 45 SOUT | 1 |
| 46 SINP |] |
| 47 SMEMR | 1 |
| 48 SHLTA | |
| 49 CLOCK (2MHz) | + |
| 50 GND | |
| PIN MNEMONIC TERM | |

| 51 | +5V | A | |
|-----------------|--|--------|---------------------------|
| 52 | -15V | B | |
| 53 | SSW DSB | tc | |
| $\frac{55}{54}$ | EXT CLR | D | X |
| 55 | EAT CLK | E | |
| 56 | | | |
| | | F | |
| 57 | | Н | _ |
| 58 | | J | |
| 59 | | K | |
| 60 | | L | |
| 61 | | М | |
| 62 | 2 | N | |
| 63 | | P | |
| 64 | | R | |
| 65 | | S | T |
| 66 | | T | |
| 67 | PHANTOM | U | |
| 68 | MWRITE | V | X |
| 69 | PS | W | |
| 70 | PROTECT | X | X |
| 71 | RUN | Y | X |
| 72 | PRDY | Z | X |
| 73 | PINT | a | X |
| 74 | PHOLD | b | X |
| 75 | PRESET | c | X |
| 76 | PSYNC | d | $\frac{\Lambda}{X}$ |
| 77 | PWR | | $\frac{\hat{x}}{\hat{x}}$ |
| 78 | PDBIN | e f | $\frac{\Lambda}{X}$ |
| 79 | AØ | h | |
| 80 | AU | | |
| 81 | A1 A2 | j | |
| | | k | |
| 82 | A6 A7 | 1 | |
| 83 | and a second sec | m | |
| 84 | A8 | n | |
| 85 | A13 | р | |
| 86 | A14 | r | |
| 87 | A11 | S | |
| 88 | DO2 | t | X |
| 89 | DO3 | u | X |
| 90 | DO7 | v | X |
| 91 | DI4 | w | X X X X X |
| 92 | D15 | x | X |
| 93 | DI6 | У | Х |
| 94 | DII | Z | |
| 95 | DIØ | AA | X |
| 96 | SINTA | AB | |
| 97 | ·SWO | AC | |
| 98 | SSTACK | AD | 1 |
| 99 | POC | AĒ | |
| 100 | GND | AF | 1 |
| | MNEMONIC | ALTER, | TERM |
| | | PIN | 1 |
| | | DESIG. | |

3

S-100 (WAMECO) BUS DESCRIPTION

| Pin | # Mnemonic | Enabled State | Description |
|--------|--------------|---------------------------------------|--|
| i | +8 Volts | NA | Unregulated +8 Volts DC. |
| | • 1 2 | | This voltage should not be |
| | | | less than +8 or greater than +11 volts. |
| 2 | +16 Volts | NA | Unregulated +16 Volts DC. |
| | | | This voltage should not be |
| | | | less than +16 or greater than +20 Volts. |
| 3 | XRDY | Low | Causes CPU to enter WAIT |
| | | | state when enabled. |
| 4 | VIO | Low | Vectored Interrupt priority 0 |
| 5 6 | VII | Low | Vectored Interrupt priority 1 |
| 6 | | Low | Vectored Interrupt priority 2 |
| 7 | VI3 | Low | Vectored Interrupt priority 3 |
| 8 | VI4 | Low | Vectored Interrupt priority 4 |
| 9 | | Low | Vectored Interrupt priority 5 |
| 10 | VIG | Low | Vectored Interrupt priority 6 |
| 11 | VI7 | Low | Vectored Interrupt priority 7 |
| 12 | | NA | Not used |
| 13 | | NA | Not used |
| 14 | | NA | Not-used |
| 15 | | NA | Not used |
| 16 | | NA | Not used |
| 17 | | NA | Not used |
| 18 | STAT DISABLE | Low | The eight status line buffers |
| | | | on the CPU board enter the |
| | | • | high impedance state when |
| | | | enabled. |
| 19 | C/C DISABLE | Low | The six command/control |
| | | | line buffers on the CPU board |
| | | | enter the high impedance |
| | 8 6 . | | state when enabled. |
| 20 | UNPROTECT | High | Combined with address in an |
| | | | AND gate on a memory board |
| | | о И | which causes the PROTECT |
| | | | flip-flop to be cleared. |
| 21 | SS | High | Indicates the CPU is single |
| | n | constant 20 | stepping. |
| 22 | ADDR DSBL | Low | The 16 address line buffers |
| | | | on the CPU board enter the |
| | | 2 | high impedance state when |
| | | | enabled. |
| 23 | DO DSBL | Low | The eight data-out lines on |
| | | | the CPU board enter the high |
| | | | impedance state when enabled. |
| 24 | Ø 2 | High | Buffered TTL CPU phase 2 |
| | | | clock. |
| 25 | Ø 1 | High | Buffered TTL CPU phase 1 |
| | N N | · · · · · · · · · · · · · · · · · · · | clock. |
| 26 | PHLDA | High | CPU board "Hold Acknowledge" |
| | | | to HOLD-H input. |
| 27 | PWAIT | High | CPU output showing a WAIT |
| | | | state is occuring. |
| | | Figure 3B. | |

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

| Pin # | Mnemonic | Enabled State | Description |
|-------|---------------|----------------|--------------------------------|
| 28 | PINTE | High | CPU output showing that |
| 8 | | | Interrupts are enabled. |
| 29 | A5 | High | Address Bit 5 |
| 30 | A4 | High | Address Bit 4 |
| 31 | A3 • | High | Address Bit 3 |
| 32 | A15 | High | Address Bit 15 |
| 33 | A12 | High | Address Bit 12 |
| 34 | A9 | High | Address Bit 9 |
| 35 | DO1 | High | CPU Data Out Bit 1 |
| 36 | DO0 | High | CPU Data Out Bit 0 |
| 37 | A10 | High | Address Bit 10 |
| 38 | DO4 | High | CPU Data Out Bit 4 |
| 39 | DO5 | High | CPU Data Out Bit 5 |
| 40 | DO6 | High | CPU Data Out Bit 6 |
| 41 | D12 | High | |
| 42 | D12 D13 | | Data In Bit 2 to CPU |
| 43 | D17 | High | Data In Bit 3 to CPU |
| 44 | SM1 | High | Data In Bit 7 to CPU |
| 11 | 51/11 | High | CPU output indicating it is |
| 45 | COLL | | performing Fetch Instruction. |
| 45 | SOUT | High | CPU output showing it is in an |
| | AT 1 D | | output cycle. |
| 46 | SINP | High | CPU output showing it is in an |
| | | | input cycle. |
| 47 | SMEMR | High | CPU status signal indicating |
| | | | the current cycle is a Memory |
| | | | Read cycle. |
| 48 | SHLTA | High | CPU status signal indicating |
| | | - | the CPU is halted. |
| 49 | CLOCK(2MHz |) Low | A buffered 2 MHz clock for |
| | | | general use. |
| 50 | GND | NA | Ground (common) |
| 51 | +8 Volts | NA | (Same as pin 1) |
| 52 | -16 Volts | NA | Unregulated-16 Volts DC. |
| | | | This voltage should not be |
| | | | greater than -16 or less than |
| | | | -20 Volts. |
| 53 | SSW DSB | Low | Sense Switch Disable disables |
| | | 2011 | |
| | | | CPU board data input buffers |
| | | | so that CPU can read sense |
| 54 | EXT CLR | Low | switches. |
| 51 | | LOW | Front panel generated I/O |
| 55 | | NT A | clear signal. |
| 56 | | NA | Not used |
| 50 | | NA | Not used |
| | | NA | Not used |
| 58 | | NA | Not used |
| 59 | | NA | Not used |
| 60 | | NA | Not used |
| 61 | | NA | Not used |
| 62 | | NA | Not used |
| 63 | | NA | Not used |
| 64 | | NA | Not used |
| 65 | | NA | Not used |
| 66 | | NA | Not used 5 |
| 67 | PHANTOM | NA | Used for Memory Bank Selection |
| | Figure | 3B (continued) | (or for SOL Systems) |
| | - | | |
| | | | |

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

a

| Pin # | Mnemonic | Enabled State | Description |
|----------|----------|--------------------|--|
| 68 | MWRITE | High | CPU output showing Data Out Bus data is to be written |
| | | | into the memory selected by |
| | | | the address lines. |
| 59 | PS | Low | Shows Protect Status of |
| | | | selected memory. |
| 0 | PROTECT | High | Combined with address in an |
| | | | AND gate on a memory boar |
| | | | which causes the PROTECT |
| | | | flip-flop to be set. |
| 71 | RUN | High | Front panel indication that |
| | | | CPU run instruction has bee |
| 70 | DDDV | T | input. |
| 72 | PRDY | Low | Causes the CPU to enter the WAIT state when enabled. |
| 73 | PINT | Low | If interrupts have been en- |
| | L TIN I | LOw | abled causes the CPU to ent |
| | | | the Interrupt Acknowledge |
| | | | condition at the conclusion of |
| | | | the current instruction. |
| 74 | PHOLD | Low | CPU input which causes a |
| | | | HOLD status to occur. DM |
| | | | transfer request signal is |
| | | | PHOLD. |
| 75 | PRESET | Low | CPU board system reset |
| - / | 201110 | | signal. |
| 76 | PSYNC | High | CPU output showing the sta |
| | | | of a new machine cycle. Th |
| | | | signal is used on the CPU board to enable the loading |
| | | | of the System Status Latch. |
| 77 | PWR | Low | Indication that data on the |
| | | | Data Out Bus is to be writte |
| | | | either to a memory or an |
| | | | I/O device. |
| 78 | PDBIN | Low | Indication to the selected |
| | | | memory or I/O device that |
| | | | the CPU expects data on the |
| 70 | • • | TT: _1_ | Data In Bus. |
| 79 80 | A0 A1 | High | Address Bit 0 Address Bit 1 |
| 81 | A2 | High High | Address Bit 1 Address Bit 2 |
| 82 | A6 | High | Address Bit 6 |
| 83 | A7 | High | Address Bit 7 |
| 84 | A8 | High | Address Bit 8 |
| 85 | A13 | High | Address Bit 13 |
| 86 | A14 | High | Address Bit 14 |
| 87 | A11 | High | Address Bit 11 |
| 88 | DO2 | High | CPU Data Out Bit 2 |
| 89 | DO3 | High | CPU Data Out Bit 3 |
| 90 | DO7 | High | CPU Data Out Bit 7 |
| 91 | DI4 | High | Data In Bit 4 to CPU |
| 92 | DI5 | High | Data In Bit 5 to CPU Data In Bit 6 to CPU |
| 93 | DI6 | High | Data III DIL 0 10 CF 0 |
| | Figu | are 3B (continued) | |
| | | | |

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

| Pin # | Mnemonic | Enabled State | Description |
|-------|----------|--|--|
| 94 | DII | High | Data In Bit 1 to CPU |
| 95 | DIO | High | Data In Bit 0 to CPU |
| 96 | SINTA | High | CPU Interrupt Acknowledge Signal |
| 97 | SWO | Low | CPU output indicating the current cycle involves writing to a memory or I/O device. |
| 98 | SSTACK | High | CPU output indicating the address bus contains the |
| | | ting the set of the se | stack address and the current cycle will have a stack operation. |
| 99 | POC | Low | Power On Clear reset signal |
| 100 | GND | NA | Ground (common) |

Figure 3B (continued)

Siz.

I-4. After inserting all connectors, place a book or other stiff object on top of the connectors. Hold the board to the book and turn them over so that the underside of the board is up.

I-5. Apply the flux to all connector pins and then solder the two end pins of each connector while pressing the board down. This will ensure that the connector is mounted flat against the board. When all the connectors have been tacked in place, finish soldering all the other pins on the connectors.

I-6. If the termination networks are to be installed, bend the leads of the resistors and capacitors so they will fit on the board. Because the resistors and capacitors are closely positioned on this board, it is suggested that their leads be bent using a simple jig. Groove a piece of 7/16'' wide wood down the center to a width equal to the length of the resistor (approximately 9/32''). Cut a shallow slot perpendicular to the resistor slot. Place the resistor so its body is in the groove with its leads in the small slots on each side. Press down on the leads (see figure 4).

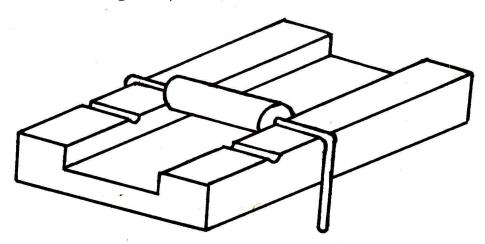


Figure 4. Lead Bending Jig

I-7. If the capacitors are axial cased, form them as detailed for the resistors. If disc capacitors are used, bend the lead as shown in figure 5. Place the disc so that it is centered over the groove and is perpendicular to the surface of the jig and bend the leads.

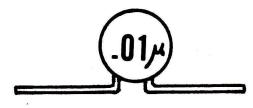


Figure 5. Disc Capacitor



Before soldering any components on the board, doublecheck to ensure that the components are placed to terminate the proper line.

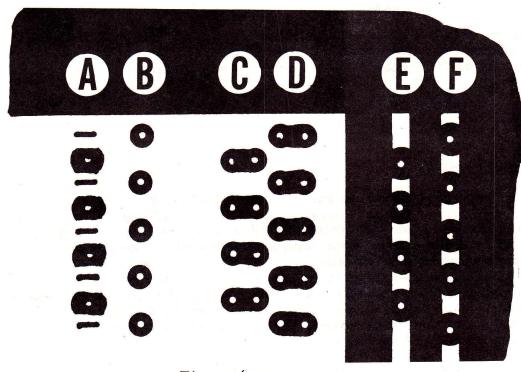


Figure 6

I-8. Place the QMB-12 motherboard component side up so that the words "component side" on the board are to the left. Compare figure 6 with the right side of the QMB-12. Rows A-F comprise the mounting points for the RC termination network for the QMB-12. Alternate rows are used, i.e. A, C, E and B, D, F. Rows B, D, F terminates pins 53-99. Rows A, C, E terminates pins 3-49.

I-9. To terminate a particular line, select the proper row (A for 3-49, B for 53-99) and count down from the top or up from the bottom the proper number of holes. Don't forget that the first pin on top is 3 or 53, the first pin on the bottom is 49 or 99.

I-10. After locating the proper hole in row A or B, find the companion set of holes in row C or D. Place one lead of a termination resistor in the proper row AB hole and the other lead in the proper right hand hole of row CD. Push the resistor fully into the board and bend the leads so the resistor will stay in place until it is soldered.

I-11. There are two rows of resistors and two rows of capacitors in the termination network. Since these rows overlap, it is easier to do one row

at a time. Finish inserting all terminationresistors in the rowstarted. Turn the board over and solder the components to the board. Clip the excess leads with the diagonal pliers. Repeat this process with the other row of resistors.

I-12. After the resistors are in place, it is easy to finish the termination. Place a capacitor lead in the left hand hole of row CD and the other lead in the corresponding hole of row EF. After each capacitor is put in place, bend the leads to hold it in place until it is soldered. Insert all termination capacitors on the row CD started. Turn the board over and solder the components to the board. Clip the excess leads with the diagonal pliers. Repeat this process with the other row of capacitors.

I-13. If regulated voltages are needed for the kluge area, install the needed regulators and tantalum capacitors as shown on figure 8, Parts Placement. Insure the polarity of the tantalums are correct when installed on the board.

I-14. When all components have been soldered in place, clean off the flux with flux cleaner.

II. Inspection and Testing

II-1. Using a strong light and the magnifying glass look at all lines and solder connections for cold solder joints, missed solder joints, solder bridges, and slivers. Correct the bad joints and missed solder joints by resoldering. If any slivers are found, cut and scrape them with an Xacto knife. Use the solder wick and soldering to remove any solder bridges found. Cover the solder bridge with flux and place a clean piece of solder wick on top of the bridge. Place the soldering iron on top of the solder wick and hold until solder is seen flowing up into the solder wick. Remove the iron and wick. Check to see if the bridge has been completely removed. If not, repeat the process until the bridge has been removed. Clean the flux off the board with flux cleaner.

II-2. Slivers are hairline traces between normal traces. These occur very infrequently on well made boards. However, if they are found cut and scrape them off the board.

II-3. When the visual inspection is completed, check the three voltage lines to ensure they are not shorted to each other or ground. If shorts are found between the voltage lines or between the voltage lines and ground, reinspect between the lines at each end of the board. It is possible there are slivers that were not detected during the earlier inspection. The next check will be for shorts between the lines. There are only two sets that should be shorted (1 to 51 and 50 to 100). The fastest way to check for shorts is to walk the probes of the multimeter (set to Rx1) down the input connections on the left hand side of the board. Before walking the probes, place the probes on +15V (pin 2) and pin 3. Check for short. Check -15V (pin 52) and pin 53 for short. To walk the probes, place the probes in the top connection in each row of the input connection points (pins 3 and 53), check for short. Move the left probe from 3 to 4. Check for short. Move the right probe from 53 to 54. Check for short. Repeat the above steps, moving the probes alternately until you have completed all pins. If any shorts are found, inspect the lines and correct the solder bridges or slivers as outlined in paragraphs II-l and II-2.

II-4. The last inspection before connection to the rest of the computer is the open test. Using the multimeter (set to $R \ge 1$), check each line from end to end. Don't try to measure between the input connection and ground if the line is terminated. The capacitor in the RC network will make the line appear as an open (infinite) resistance. In all cases, measure between the input connection and the left hand side of the RC network line. If an open is found, cut a short piece of solid copper wire, apply flux to the area of the open circuit and solder the wire across the open. Clean the area with flux cleaner and recheck.

II-5. The QMB-12 is now ready to be connected to the rest of the computer. The top power lead is -15V, the center is +8V, and the bottom is +15V.

There are six ground points on the input side of the board. Multiple grounds should be applied from different points in the computer. Use the largest wire that will fit in the holes.

II-6. When connecting circuit wires to the QMB-12, double check before connecting each one that the wire is the correct one for the hole.

III. General

III-1. The Kluge area on the lower right side of the QMB-12 is provided for experimental purposes. There are six ground points plus multiple connection points for the three regulated voltages that may be hardwired to for power.

III-2. This Wameco product is guaranteed for a period of 90 days from date of purchase from your dealer against defects in manufacturing. Upon receipt of the defective board by Wameco Incorporated, prepaid freight or mailing, the defective board will be cheerfully replaced. The guaranty is limited to replacement of the board (and parts if parts were supplied by Wameco) even though the board may be defective through negligence in manufacturing or through other fault.

III-3. For reference front and rear photos of the QMB-12 board before parts installation are furnished (see figures 7A, 7B).

III-4. We sincerely hope that the QUIET MOTHER_{TM} will give you long and satisfactory service. If you have any problems with the QMB-12, or if you just want to comment on the board, please write to me personally.

Jorn Watters

Norm Walters President Wameco Inc. 3107 Laneview Drive San Jose, Ca. 95132

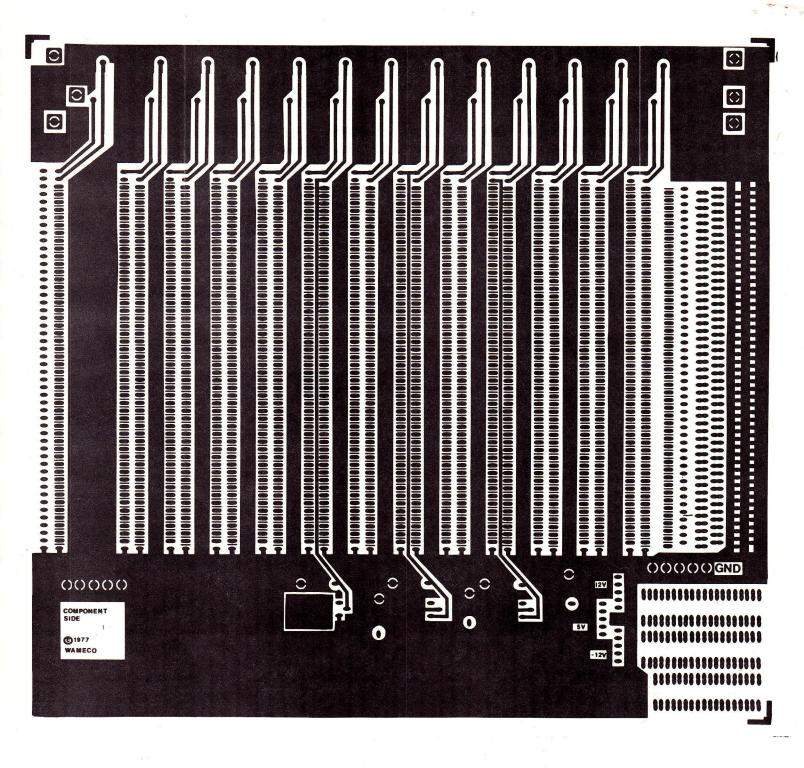
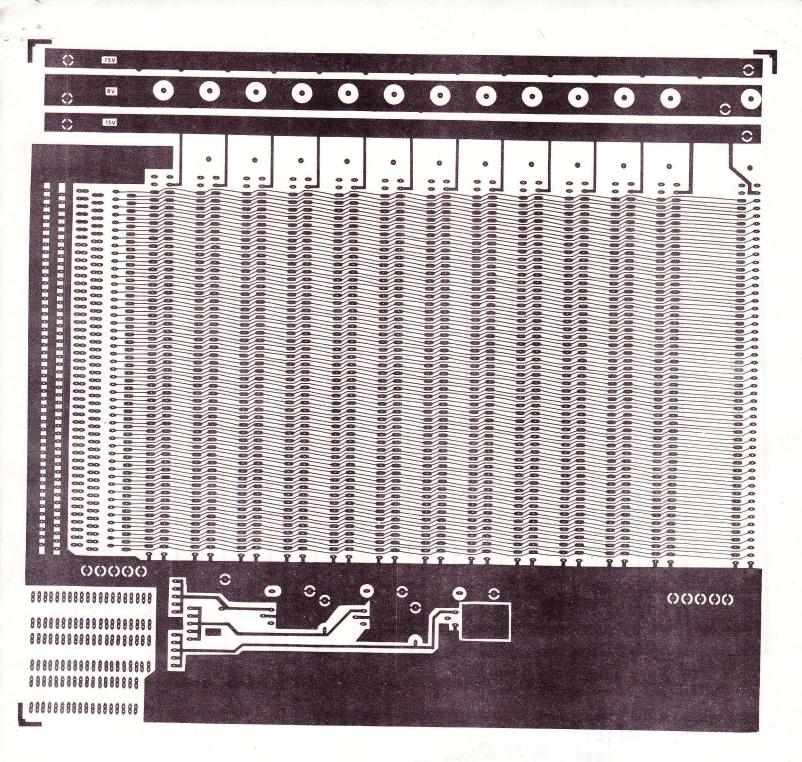
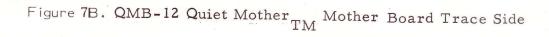


Figure 7A. QMB-12 Quiet Mother TM Mother Board Component Side





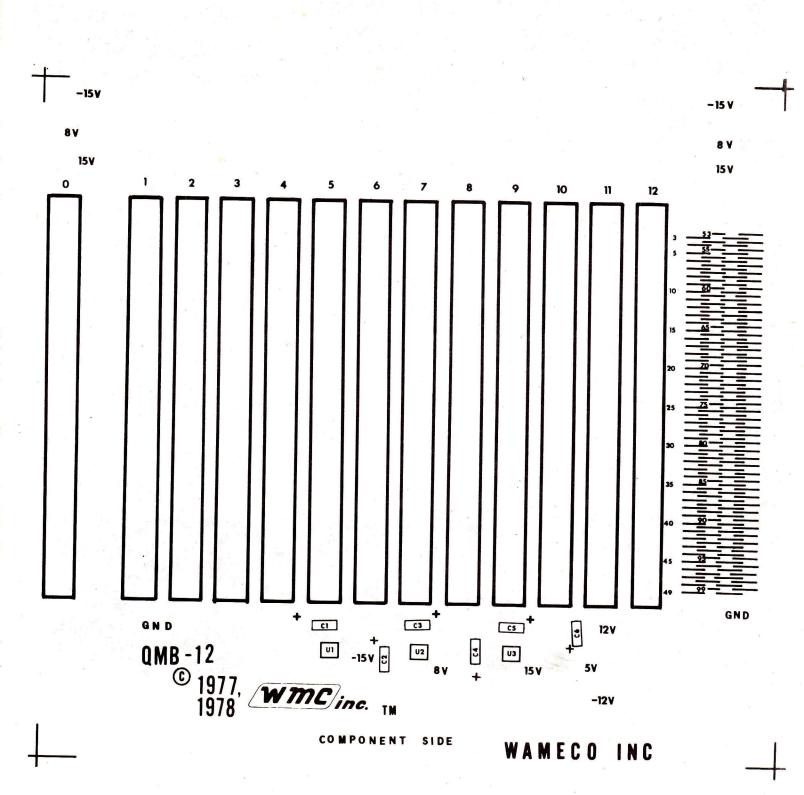


Figure 8. QMB-12 Parts Placement